Data Sheet | December 8, 2006 | FN6390.0

Dual Micropower, Single Supply, Rail-to-Rail Input and Output (RRIO) Instrumentation Amplifier

The ISL28271 and ISL28272 are dual micropower instrumentation amplifiers (in-amps) optimized for low 2.4V to 5V single supplies.

Both devices feature an Input Range Enhancement Circuit (IREC) which maintains CMRR performance for input voltages equal to the positive and negative supply rails. The input signal is capable of swinging 10% above the positive supply rail and to 100mV below the negative supply with only a slight degradation of the CMRR performance. The output operation is rail to rail.

The ISL28271 is compensated for a minimum gain of 10 or more. For higher gain applications, the ISL28272 is compensated for a minimum gain of 100. The in-amps have CMOS input devices for maximum input common voltage range. The amplifiers can be operated from one lithium cell or two Ni-Cd batteries.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28271FAZ (Note)	28271 FAZ	97/Tube	16 Ld QSOP (Pb-free)	MDP0040
ISL28271FAZ-T7 (Note)	28271 FAZ	7” (1000 pcs)	16 Ld QSOP (Pb-free)	MDP0040
ISL28272FAZ (Note)	28272 FAZ	97/Tube	16 Ld QSOP (Pb-free)	MDP0040
ISL28272FAZ-T7 (Note)	28272 FAZ	7” (1000 pcs)	16 Ld QSOP (Pb-free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

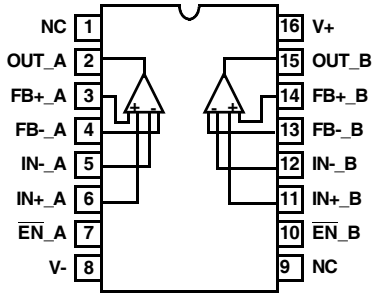
- 120µA typical supply current for both channels
- 30pA max input bias current
- 100dB CMRR, PSRR
- 0.7µV/°C offset voltage temperature coefficient
- 180kHz 3dB Bandwidth - ISL28271
- 100kHz 3dB Bandwidth - ISL28272
- 0.5V/µs slew rate
- Single supply operation
- Rail-to-rail input and output (RRIO)
- Input is capable of swinging above V+ and below V- (ground sensing)
- 0.081%1 typical gain error - ISL28271
- -0.19%1 typical gain error - ISL28272
- Pb-free plus anneal available (RoHS compliant)

Applications

- Battery- or solar-powered systems
- Strain gauge
- Sensor signal conditioning
- Medical devices
- Industrial instrumentations

Pinout

ISL28271, ISL28272
(16 LD QSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V
Supply Turn On Voltage Slew Rate 1V/µs
Input Current (IN, FB) ISL28272 . . . . . 5mA
Differential Input Voltage (IN, FB) ISL28272 . . . . . 0.5V
Input Current (IN, FB) ISL28271 . . . . . 5mA
Differential Input (IN, FB) Voltage ISL28271 . . . . . 1.0V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD tolerance, Human Body Model 3kV
ESD tolerance, Machine Model 300V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
16 Ld QSOP Package	112

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V+ = +5V, V- = GND, V_{FB+} = 1/2V+, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C**.

PARAMETER	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	ISL28271		-600 **-1200**	±35	600 **1200**	µV
		ISL28272		-500 **-750**	±35	500 **750**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient -40°C to +125°C				0.7		µV/°C
I_{OS}	Input Offset Current between IN+ and IN-, and between FB+ and FB-	See graphs for extended temperature range -40°C to +85°C		-30 **-80**	±5	30 **80**	pA
I_B	Input Bias Current (IN+, IN-, FB+, and FB- terminals)	See graphs for extended temperature range -40°C to +85°C		-30 **-80**	±10	30 **80**	pA
e_N	Input Noise Voltage	ISL28271	f = 0.1Hz to 10Hz		10		μV_{P-P}
		ISL28272			6		μV_{P-P}
	Input Noise Voltage Density	ISL28271	f_0 = 1kHz		240		nV/√Hz
		ISL28272			78		nV/√Hz
i_N	Input Noise Current Density	ISL28271	f_0 = 1kHz		0.92		pA/√Hz
		ISL28272			0.2		pA/√Hz
R_{IN}	Input Resistance				1		GΩ
V_{IN}	Input Voltage Range	V+ = 2.4V to 5.0V		0		V+	V
CMRR	Common Mode Rejection Ratio	ISL28271	V_{CM} = 0V to 5V	80 **70**	100		dB
		ISL28272		80 **75**	100		dB
PSRR	Power Supply Rejection Ratio	V+ = 2.4V to 5V		80 **75**	100		dB
E_G	Gain Error	ISL28271	R_L = 100kΩ to 2.5V		+0.081		%
		ISL28272			-0.19		

Electrical Specifications V+ = +5V, V- = GND, V_{FB+} = 1/2V+, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Maximum Voltage Swing	Output low, R_L = 100kΩ			3	6 **30**	mV
		Output low, R_L = 1kΩ			130	175 **225**	mV
		Output high, R_L = 100kΩ		4.980 **4.980**	4.99		V
		Output high, R_L = 1kΩ		4.85 **4.80**	4.88		V
SR	Slew Rate	R_L = 1kΩ to GND		0.4 **0.35**	0.5	0.7 **0.75**	V/µs
-3db BW	-3dB Bandwidth	R_L = 10kΩ	ISL28271		180		kHz
			ISL28272		100		kHz
$I_{S,EN}$	Supply Current, Enabled	Both A and B channels enabled, $\overline{EN}$ = V-			120	156 **200**	µA
$I_{S,DIS}$	Supply Current, Disabled	Both A and B channels disabled, $\overline{EN}$ = V+			4	7 **9**	µA
V_{INH}	$\overline{EN}$ Enable Pin High Level			**2**			V
V_{INL}	$\overline{EN}$ Enable Pin Low Level					**0.8**	V
I_{ENH}	$\overline{EN}$ Input Current High	$\overline{EN}$ = V+			0.8	1 **1.3**	µA
I_{ENL}	$\overline{EN}$ Input Current Low	$\overline{EN}$ = V-			26	50 **100**	nA
V+	Minimum Supply Voltage			**2.4**			V
I_{SC+}	Short Circuit Output Current	V+ = 5V, R_L = 10Ω		28 **25**	31		mA
I_{SC-}	Short Circuit Output Current	V+ = 5V, R_L = 10Ω		24 **20**	26		mA

Typical Performance Curves

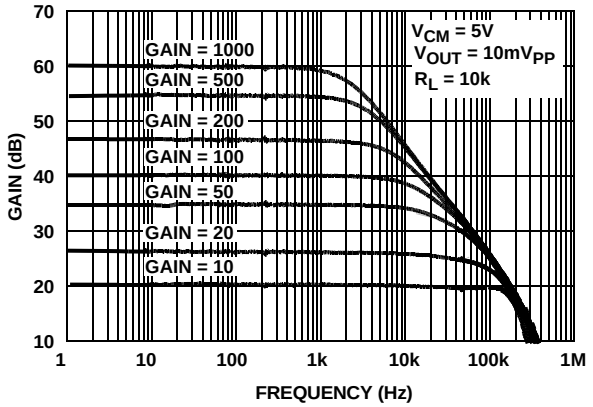


FIGURE 1. ISL28271 FREQUENCY RESPONSE vs CLOSED LOOP GAIN. V+ = V_{CM} = 5V

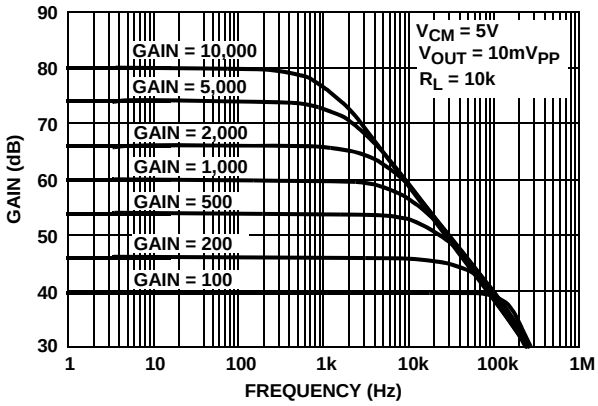


FIGURE 2. ISL28272 FREQUENCY RESPONSE vs CLOSED LOOP GAIN. V_{CM} = V+

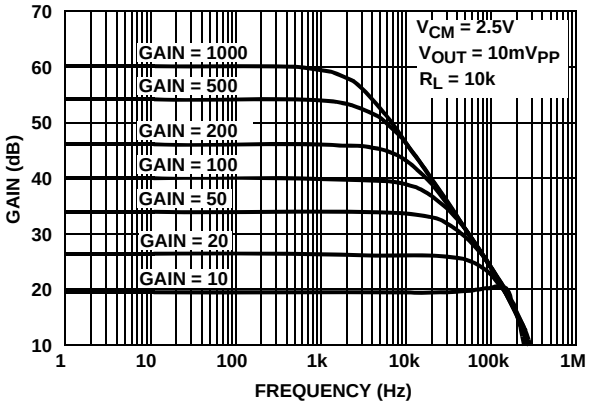


FIGURE 3. ISL28271 FREQUENCY RESPONSE vs CLOSED LOOP GAIN. V+ = 5V, V_{CM} = 1/2V+

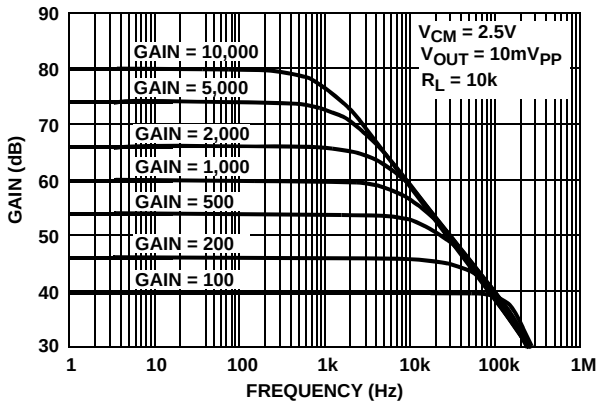


FIGURE 4. ISL28272 FREQUENCY RESPONSE vs CLOSED LOOP GAIN. V_{CM} = 1/2V+

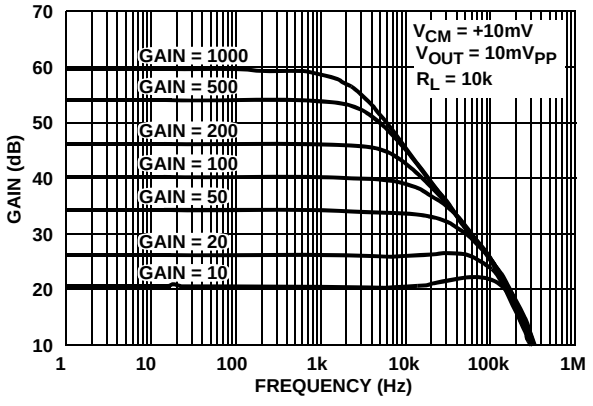


FIGURE 5. ISL28271 FREQUENCY RESPONSE vs CLOSED LOOP GAIN. V+ = 5V, V_{CM} = 10mV

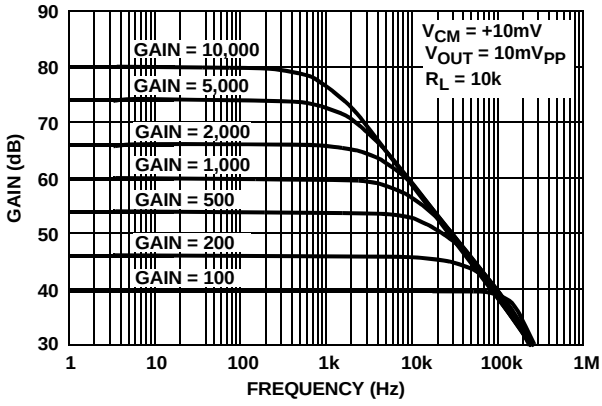


FIGURE 6. ISL28272 FREQUENCY RESPONSE vs CLOSED LOOP GAIN. V_{CM} = V-

Typical Performance Curves (Continued)

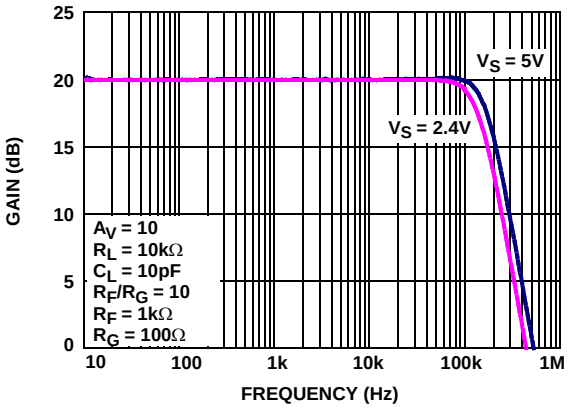


FIGURE 7. ISL28271 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

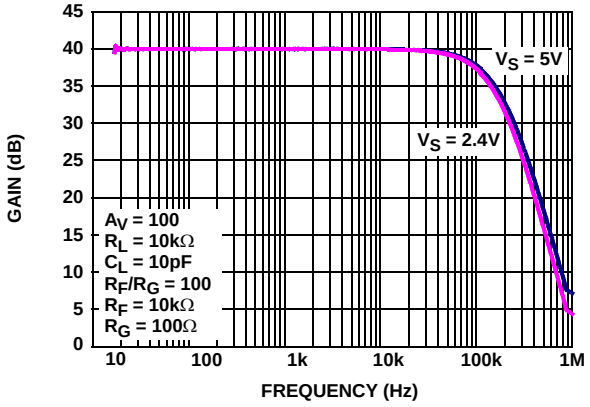


FIGURE 8. ISL28272 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

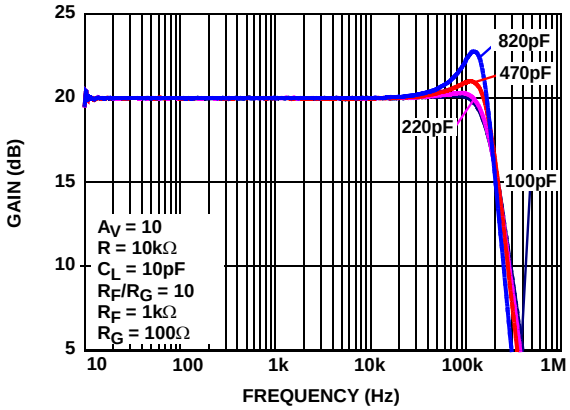


FIGURE 9. ISL28271 FREQUENCY RESPONSE vs C_{LOAD}

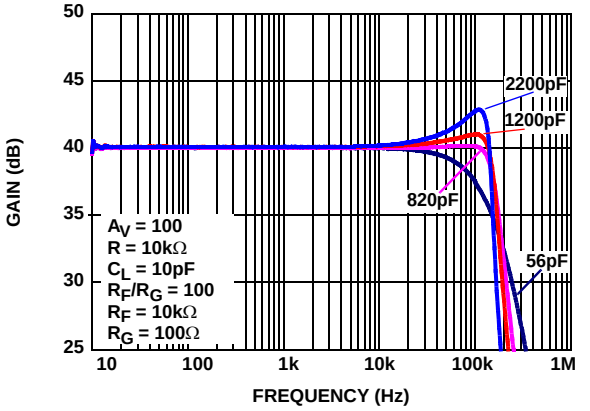


FIGURE 10. ISL28272 FREQUENCY RESPONSE vs C_{LOAD}

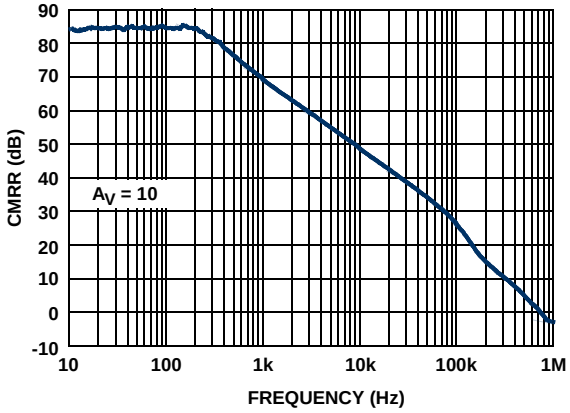


FIGURE 11. ISL28271 CMRR vs FREQUENCY

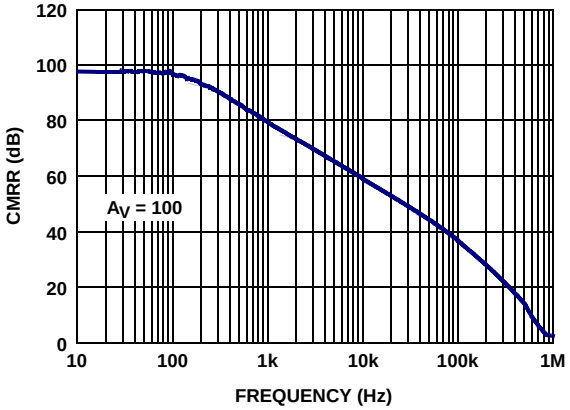


FIGURE 12. ISL28272 CMRR vs FREQUENCY

Typical Performance Curves (Continued)

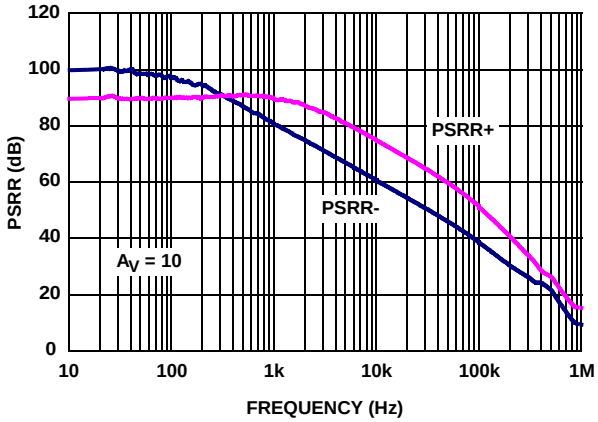


FIGURE 13. ISL28271 PSRR vs FREQUENCY

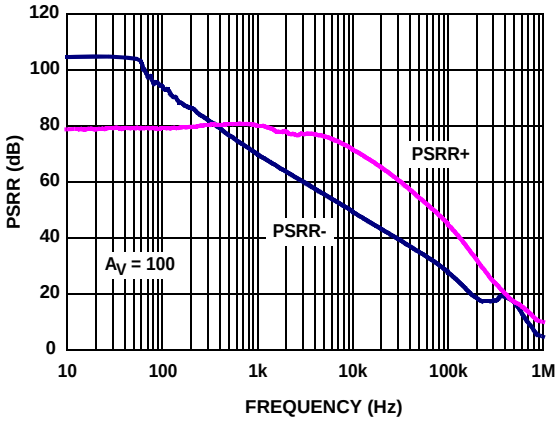


FIGURE 14. ISL28272 PSRR vs FREQUENCY

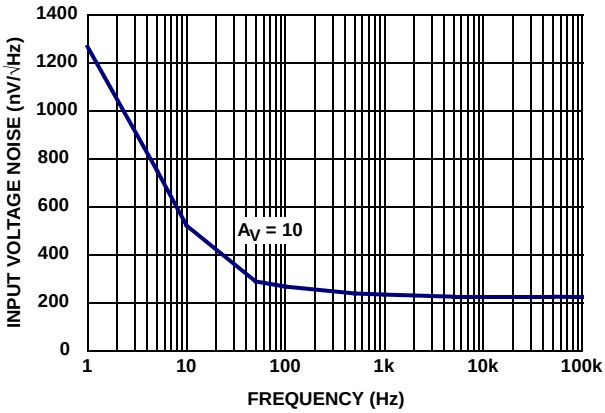


FIGURE 15. ISL28271 INPUT VOLTAGE NOISE SPECTRAL DENSITY

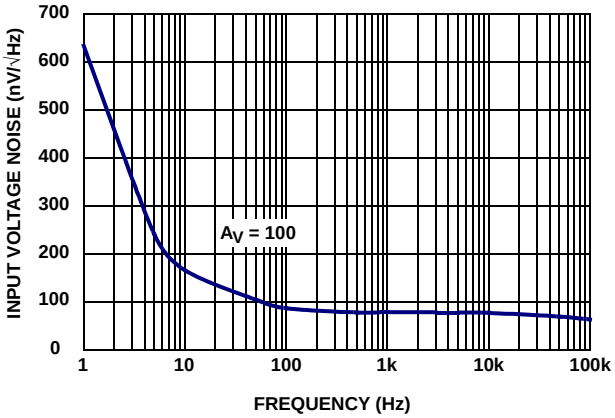


FIGURE 16. ISL28272 INPUT VOLTAGE NOISE SPECTRAL DENSITY

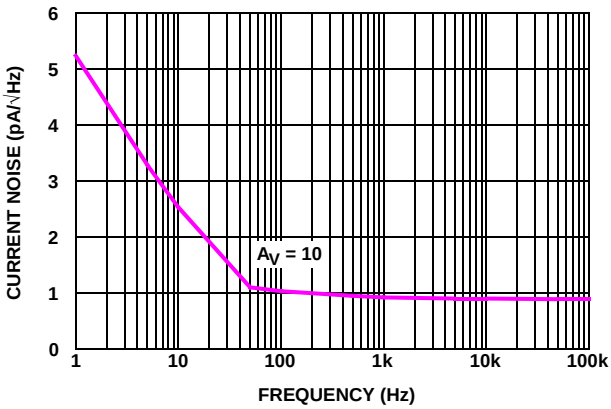


FIGURE 17. ISL28271 INPUT CURRENT NOISE SPECTRAL DENSITY

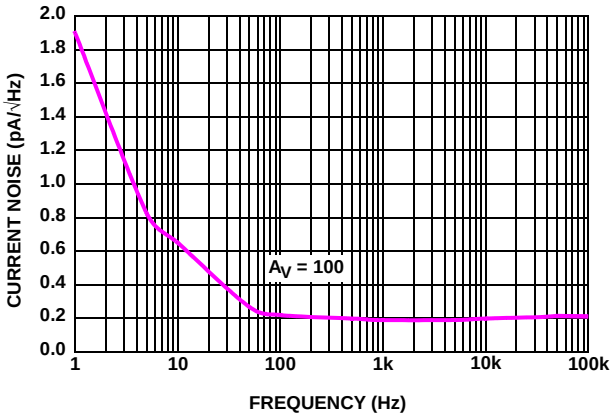


FIGURE 18. ISL28272 INPUT CURRENT NOISE SPECTRAL DENSITY

Typical Performance Curves (Continued)

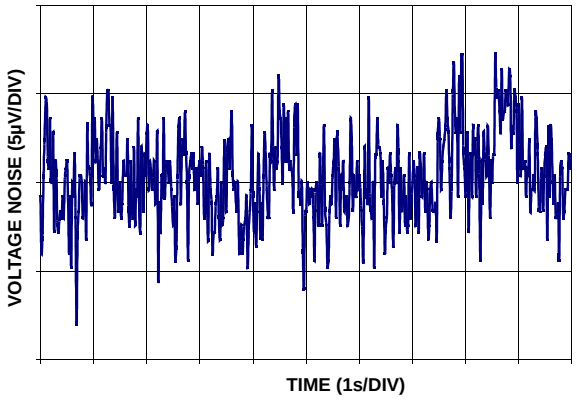


FIGURE 19. ISL28271 0.1 Hz TO 10Hz INPUT VOLTAGE NOISE. GAIN = 10

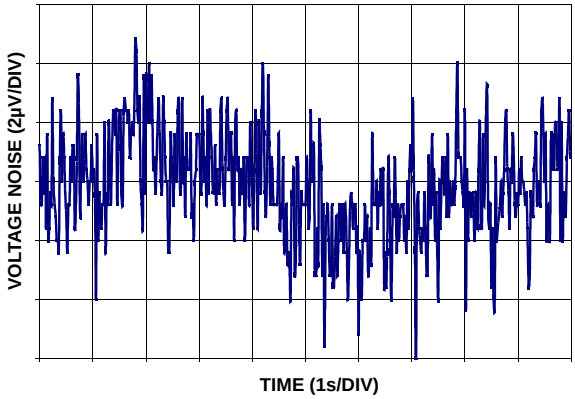


FIGURE 20. ISL28272 0.1 Hz TO 10Hz INPUT VOLTAGE NOISE. GAIN = 100

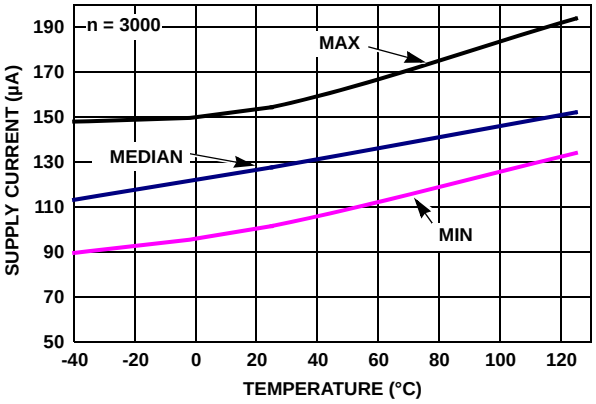


FIGURE 21. ISL28271 SUPPLY CURRENT ENABLED vs TEMPERATURE V_S = ±2.5V, V_{IN} = 0V

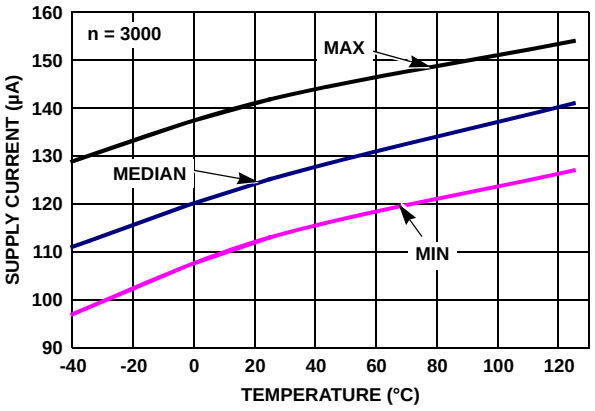


FIGURE 22. ISL28272 SUPPLY CURRENT ENABLED vs TEMPERATURE V_S = ±2.5V, V_{IN} = 0V

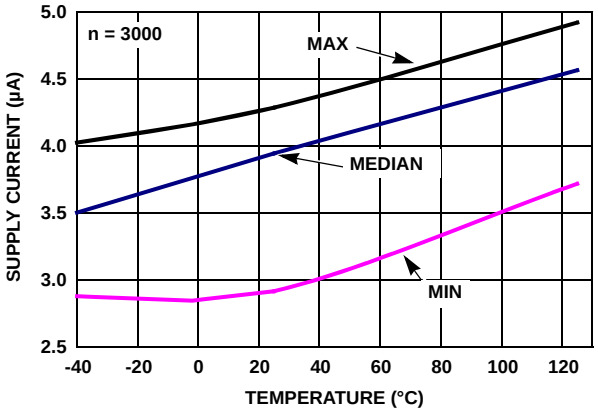


FIGURE 23. ISL28271 SUPPLY CURRENT DISABLED vs TEMPERATURE V_S = ±2.5V, V_{IN} = 0V

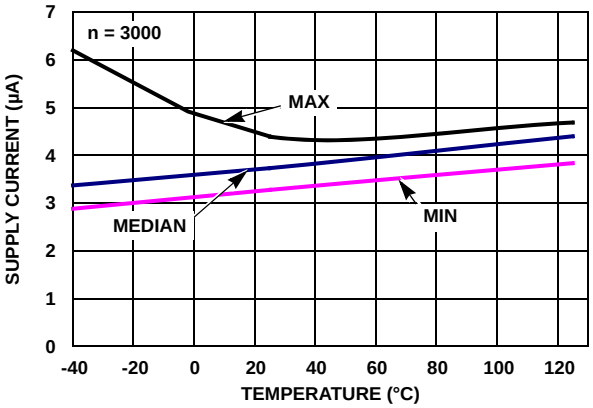


FIGURE 24. ISL28272 SUPPLY CURRENT DISABLED vs TEMPERATURE V_S = ±2.5V, V_{IN} = 0V

Typical Performance Curves (Continued)

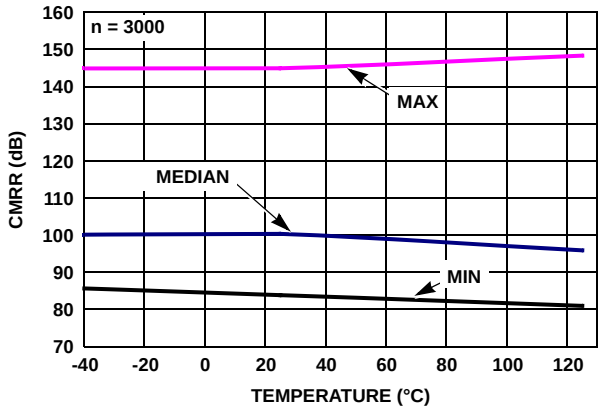


FIGURE 25. ISL28271 CMRR vs TEMPERATURE V_{CM} = +2.5V TO -2.5V

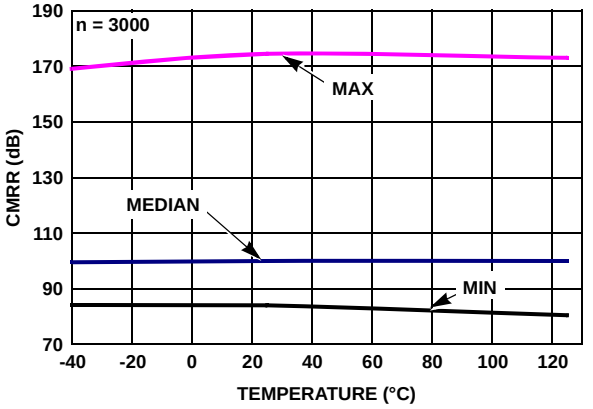


FIGURE 26. ISL28272 CMRR vs TEMPERATURE V_{CM} = +2.5V TO -2.5V

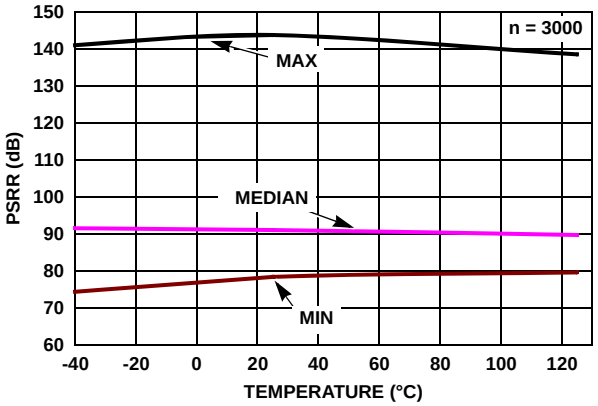


FIGURE 27. ISL28271 PSRR vs TEMPERATURE V_S = ±1.2V TO ±2.5V

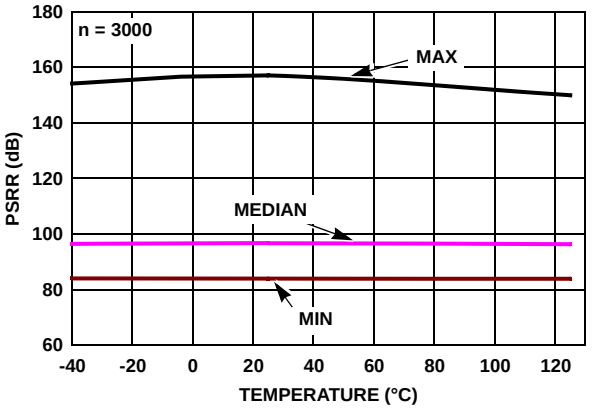


FIGURE 28. ISL28272 PSRR vs TEMPERATURE V_S = ±1.2V TO ±2.5V

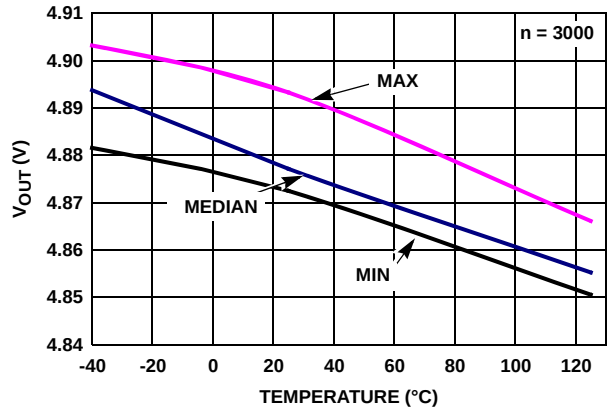


FIGURE 29. ISL28271 V_{OUT} HIGH vs TEMPERATURE R_L = 1k, V_S = ±2.5V

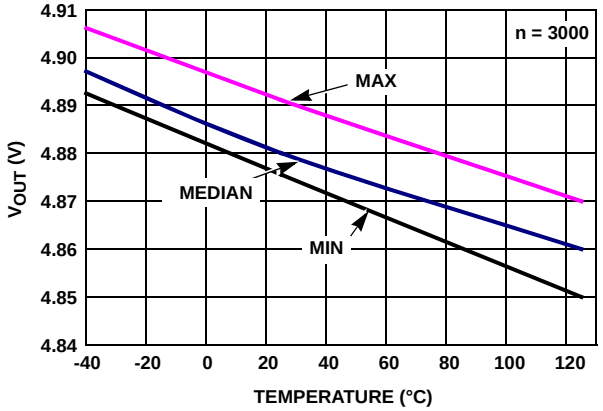


FIGURE 30. ISL28272 V_{OUT} HIGH vs TEMPERATURE R_L = 1k, V_S = ±2.5V

Typical Performance Curves (Continued)

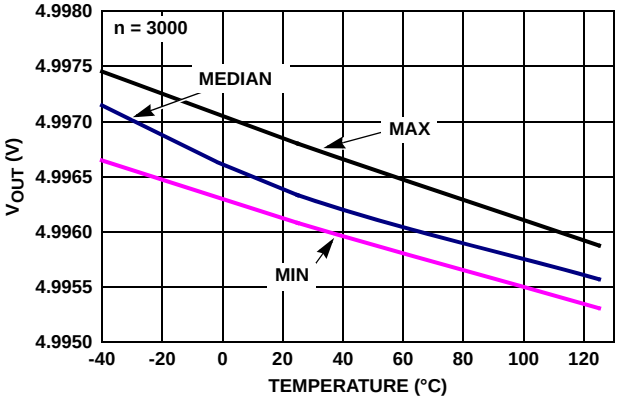


FIGURE 31. ISL28271 V_{OUT} HIGH vs TEMPERATURE R_L = 100k, V_S = ±2.5V

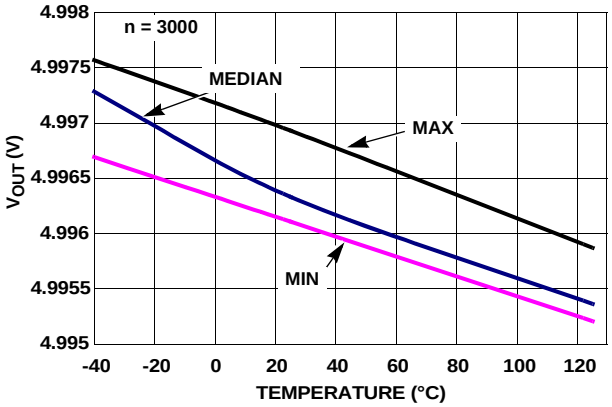


FIGURE 32. ISL28272 V_{OUT} HIGH vs TEMPERATURE R_L = 100k, V_S = ±2.5V

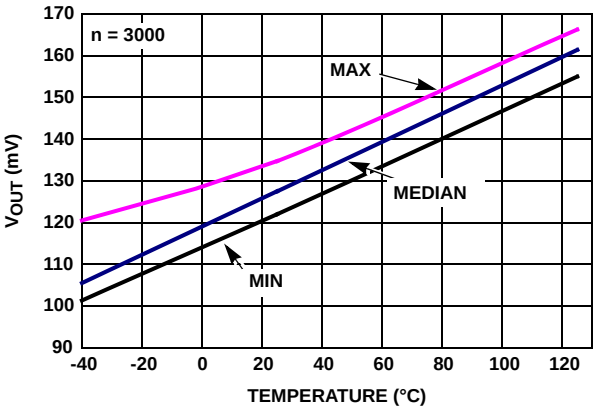


FIGURE 33. ISL28271 V_{OUT} LOW vs TEMPERATURE R_L = 1k, V_S = ±2.5V

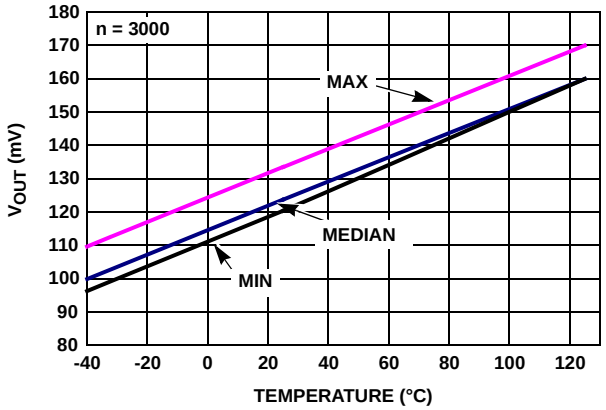


FIGURE 34. ISL28272 V_{OUT} LOW vs TEMPERATURE R_L = 1k, V_S = ±2.5V

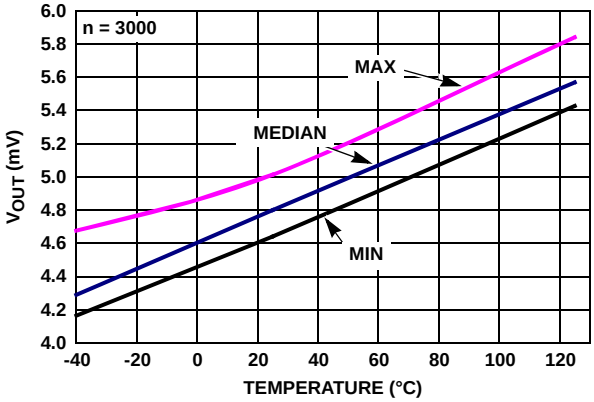


FIGURE 35. ISL28271 V_{OUT} LOW vs TEMPERATURE R_L = 100k, V_S = ±2.5V

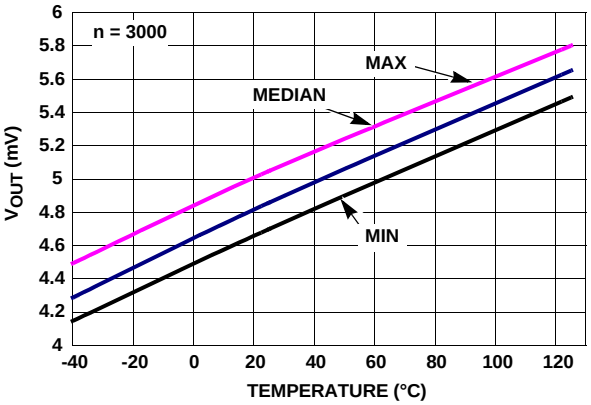
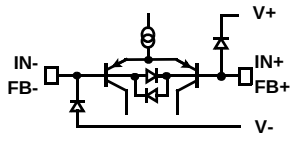


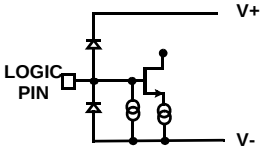
FIGURE 36. ISL28272 V_{OUT} LOW vs TEMPERATURE R_L = 100k, V_S = ±2.5V

Pin Descriptions

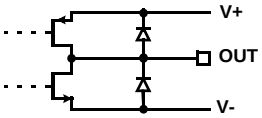
ISL28271 16 Ld QSOP	ISL28272 16 Ld QSOP	PIN NAME	EQUIVALENT CIRCUIT	PIN FUNCTION
2, 15	2, 15	OUT_A,B	Circuit 3	Output Voltage. A complementary Class AB common-source output stage drives the output of each channel. When disabled, the outputs are in a high impedance state.
3, 14	3, 14	FB+_A,B	Circuit 1A, Circuit 1B	Positive Feedback high impedance terminals. ISL28272 input circuit is shown in Circuit 1A, and the ISL28271 input circuit is shown in Circuit 1B. ISL28271: to avoid offset drift, it is recommended that the terminals of the ISL28271 are not overdriven beyond 1V and the input current must never exceed 5mA.
4, 13	4, 13	FB-_A,B	Circuit 1A, Circuit 1B	Negative Feedback high impedance terminals. The FB- pins connect to an external resistor divider to individually set the desired gain of the in-amp. ISL28272 input circuit is shown in Circuit 1A, and the ISL28271 input circuit is shown in Circuit 1B. ISL28271: to avoid offset drift, it is recommended that the terminals of the ISL28271 are not overdriven beyond 1V and the input current must never exceed 5mA.
5, 12	5, 12	IN-_A,B	Circuit 1A, Circuit 1B	High impedance Inverting input terminals. Connect to the low side of the input source signal. ISL28272 input circuit is shown in Circuit 1A, and the ISL28271 input circuit is shown in Circuit 1B. ISL28271: to avoid offset drift, it is recommended that the terminals of the ISL28271 are not overdriven beyond 1V and the input current must never exceed 5mA.
6, 11	6, 11	IN+_A,B	Circuit 1A, Circuit 1B	High impedance Non-inverting input terminals. Connect to the high side of the input source signal. ISL28272 input circuit is shown in Circuit 1A, and the ISL28271 input circuit is shown in Circuit 1B. ISL28271: to avoid offset drift, it is recommended that the terminals of the ISL28271 are not overdriven beyond 1V and the input current must never exceed 5mA.
7, 10	7, 10	$\overline{EN}$_A,B	Circuit 2	Active LOW logic pins. When pulled above 2V, the corresponding channel turns off and OUT is high impedance. A channel is enabled when pulled below 0.8V. Built-in pull downs define each $\overline{EN}$ pin LOW when left floating.
16	16	V+	Circuit 4	Positive Supply terminal shared by all channels.
8	8	V-	Circuit 4	Negative Supply terminal shared by all channels. Grounded for single supply operation.
1, 9	1, 9	NC		No Connect, pins can be left floating or grounded.



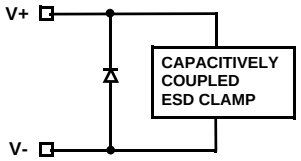
CIRCUIT 1A



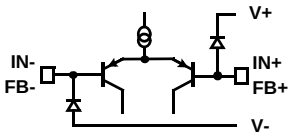
CIRCUIT 2



CIRCUIT 3



CIRCUIT 4



CIRCUIT 1B

Application Information

Product Description

The ISL28271 and ISL28272 are dual channel micropower instrumentation amplifiers (in-amps) which deliver rail-to-rail input amplification and rail-to-rail output swing. The in-amps also deliver excellent DC and AC specifications while consuming only about 120µA for both channels. Because the independent pair of feedback terminals set the gain and adjust the output zero level, the ISL28271 and ISL28272 achieve high CMRR regardless of the tolerance of the gain setting resistors. The ISL28271 is internally compensated for a minimum gain of 10. The ISL28272 is internally compensated for a minimum gain of 100.

$\overline{EN}$ pins are available to independently enable or disable a channel. When all channels are off, current consumption is down to typically 4µA.

Input Protection

All input terminals and feedback terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Input signals originating from low impedance sources should have current limiting resistors in series with the IN+ and IN- pins to prevent damaging currents during power supply sequencing and other transient conditions. The ISL28272 has additional back-to-back diodes across the input terminals and also across the feedback terminals. If overdriving the inputs is necessary, the external input current must never exceed 5mA. External series resistors may be used as an external protection to limit excessive external voltage and current from damaging the inputs. On the other hand, the ISL28271 has no clamps to limit the differential voltage on the input terminals allowing higher differential input voltages at lower gain applications. It is recommended however, that the terminals of the ISL28271 are not overdriven beyond 1V to avoid offset drift.

Input Stage and Input Voltage Range

The input terminals (IN+ and IN-) of the in-amps are a single differential pair of CMOS devices aided by an Input Range Enhancement Circuit, IREC, to increase the headroom of operation of the common-mode input voltage. The feedback terminals (FB+ and FB-) also have a similar topology. As a result, the input common-mode voltage range is rail-to-rail regardless of the feedback terminal settings and regardless of the gain settings. They are able to handle input voltages that are at or slightly beyond the supply and ground sensing making these in-amps well suited for single 5V down to 2.4V supply systems.

The IREC enables rail-to-rail input amplification without the problems usually associated with the dual differential stage topology. The IREC ensures that there are no drastic changes in offset voltage over the entire range of the input. See Input Offset Voltage vs Common-Mode Input Voltage in performance charts. IREC also cures the abrupt change and even reverse polarity of the input bias current over the whole range of input.

Output Stage and Output Voltage Range

A Class AB common-source output stage drives the output. The pair of complementary MOSFET devices drive the output VOUT to within a few millivolts of the supply rails. At a 100kΩ load, the PMOS sources current and pulls the output up to 4mV below the positive supply. The NMOS sinks current and pulls the output down to 4mV above the negative supply, or ground in the case of a single supply operation. The current sinking and sourcing capability are internally limited to 31mA. When disabled, the outputs are in a high impedance state.

Gain Setting

VIN, the potential difference across IN+ and IN-, is replicated (less the input offset voltage) across FB+ and FB-. The function of the in-amp is to maintain the differential voltage across FB- and FB+ equal to IN+ and IN-; (FB- - FB+) = (IN+ - IN-). Consequently, the transfer function can be derived. The in-amp gain is set by two external resistors, the feedback resistor RF, and the gain resistor RG.

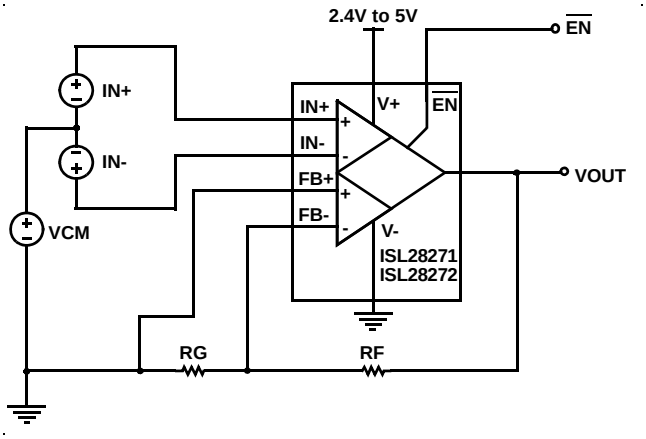


FIGURE 37. GAIN IS SET BY TWO EXTERNAL RESISTORS, R_F AND R_G

$$VIN = IN+ - IN-$$

$$VOUT = \left(1 + \frac{R_F}{R_G}\right) VIN \quad \text{(EQ. 1)}$$

In Figure 37, the FB+ pin and one end of resistor RG are connected to GND. With this configuration, the above gain equation (Equation 1) is only true for a positive swing in VIN; negative input swings will be ignored because the output will be at ground.

Reference Connection

Unlike a three op-amp in-amp realization, a finite series resistance seen at the REF terminal does not degrade the high CMRR performance eliminating the need for an

additional external buffer amplifier. Figure 38 uses the FB+ pin to provide a high impedance REF terminal.

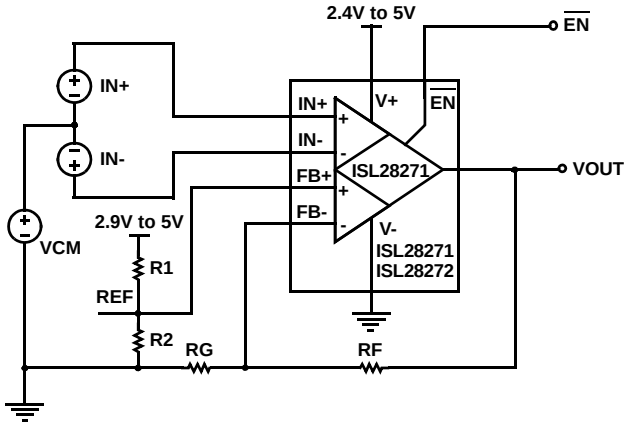


FIGURE 38. GAIN SETTING AND REFERENCE CONNECTION

$$VIN = IN+ - IN-$$

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)(VIN) + \left(1 + \frac{R_F}{R_G}\right)(VREF) \quad \text{(EQ. 2)}$$

The FB+ pin is used as a REF terminal to center or to adjust the output. Because the FB+ pin is a high impedance input, an economical resistor divider can be used to set the voltage at the REF terminal without degrading or affecting the CMRR performance. Any voltage applied to the REF terminal will shift VOUT by VREF times the closed loop gain, which is set by resistors RF and RG. See Figure 38.

The FB+ pin can also be connected to the other end of resistor, RG. See Figure 39. Keeping the basic concept that the in-amp maintains constant differential voltage across the input terminals and feedback terminals (FB- - FB+) = (IN+ - IN-), the transfer function of Figure 39 can be derived.

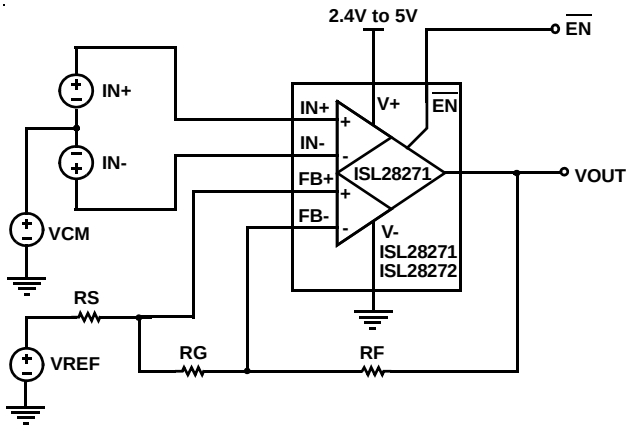


FIGURE 39. REFERENCE CONNECTION WITH AN AVAILABLE VREF

$$VIN = IN+ - IN-$$

$$VOUT = \left[1 + \frac{R_S + R_F}{R_G}\right] + VREF \quad \text{(EQ. 3)}$$

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)(VIN) + (VREF) \quad \text{(EQ. 4)}$$

A finite resistance RS in series with the VREF source, adds an output offset of VIN*(RS/RG). As the series resistance RS approaches zero, Equation 3 is simplified to Equation 4 for Figure 39. VOUT is simply shifted by an amount VREF.

External Resistor Mismatches

Because of the independent pair of feedback terminals provided by the in-amps, the CMRR is not degraded by any resistor mismatches. Hence, unlike a three op-amp and especially a two op-amp in-amp realization, the ISL28271 and ISL28272 reduce the cost of external components by allowing the use of 1% or more tolerance resistors without sacrificing CMRR performance. The CMRR will be typically 110dB regardless of the tolerance of the resistors used. Instead, a resistor mismatch results in a higher deviation from the theoretical gain - Gain Error.

Gain Error and Accuracy

The gain error indicated in the electrical specifications table is the inherent gain error alone. The gain error specification listed does not include the gain error contributed by the resistors. There is an additional gain error due to the tolerance of the resistors used. The resulting non-ideal transfer function effectively becomes:

$$VOUT = \left(1 + \frac{R_F}{R_G}\right) \times [1 \pm (E_{RG} + E_{RF} + E_G)] \times VIN \quad \text{(EQ. 5)}$$

Where:

ERG = Tolerance of RG

ERF = Tolerance of RF

EG = Gain Error of the ISL28271

The term [1 - (ERG +ERF +EG)] is the deviation from the theoretical gain. Thus, (ERG +ERF +EG) is the total gain error. For example, if 1% resistors are used, the total gain error would be:

$$TotalGainError = \pm(E_{RG} + E_{RF} + E_G(typical))$$

$$TotalGainError = \pm(0.01 + 0.01 + 0.005) = \pm 2.5\%$$

Disable/Power-Down

The ISL28271 and ISL28272 have an enable/disable pin for each channel. They can be powered down to reduce the supply current to typically 4µA when all channels are off. When disabled, the corresponding output is in a high impedance state. The active low $\overline{EN}$ pin has an internal pull down and hence can be left floating and the in-amp enabled by default. When the $\overline{EN}$ is connected to an external logic,

the in-amp will shutdown when $\overline{EN}$ pin is pulled above 2V, and will power up when $\overline{EN}$ bar is pulled below 0.8V.

Unused Channels

The ISL28271and ISL28272 are Dual channel op-amps. If the application only requires one channel when using the ISL28271 or ISL28272, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to configure the feedback pins (FB+, FB-) with the minimum gain stable values for the amplifier with RF and RG resistors and tieing the input terminals to ground (as shown in Figure 40).

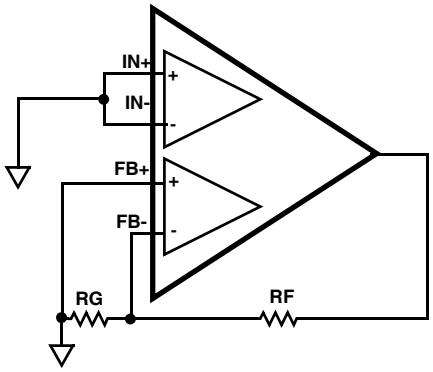
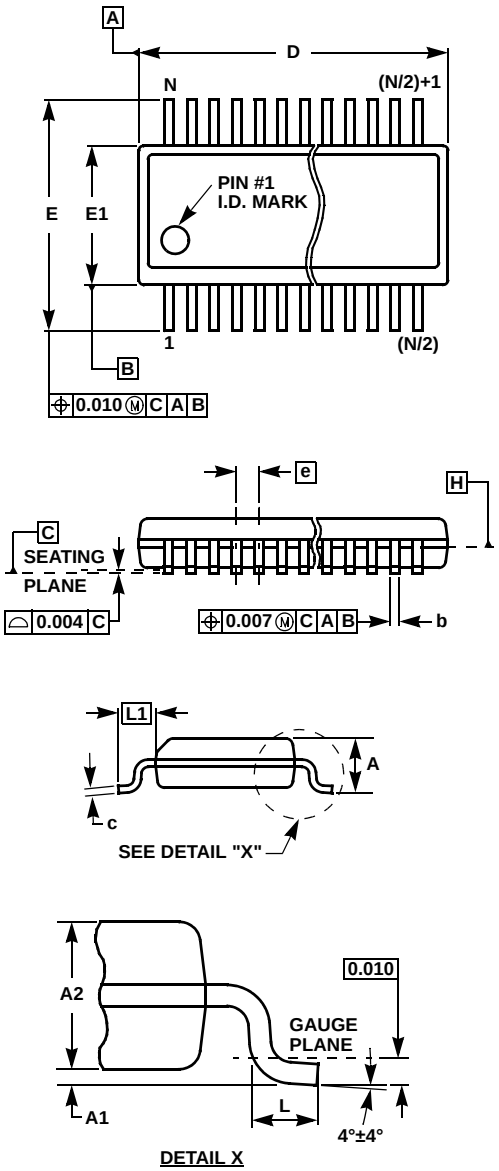


FIGURE 40. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	QSOP16	QSOP24	QSOP28	TOLERANCE	NOTES
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. E 3/01

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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